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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,706	07/29/2004	Matthew S. Angyal	FIS920040028US1	4705

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EXAMINER	
HARRISON, MONICA D	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 02/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,706	ANGYAL ET AL.	
	Examiner	Art Unit	
	Monica D. Harrison	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's amendment filed 8/31/05 has been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen et al (6,399,486 B1).

2. Regarding claim 1, Chen et al discloses a method of preventing exposure of at least one layer of a semiconductor device, the method comprising the steps of: etching through an interlevel dielectric (ILD) layer (Figure 2, reference 4) and partially into an underlying cap layer (Figure 2, reference 6) thereby leaving an opening through the ILD layer and a remaining portion of an the underlying cap layer; maintaining the semiconductor device in an inert gas (column 7, lines 32-40); and forming a portion of a liner in the opening to prevent exposure of the ILD layer during subsequent processing (Figure 3, reference 16).

3. Regarding claim 2, Chen et al discloses wherein the remaining portion is no less than approximately 10% of the underlying cap layer thickness and no greater than approximately 90% of the underlying cap layer thickness (Figure 2, reference 6).

4. Regarding claim 3, Chen et al discloses wherein the portion of the liner is no less than approximately 5% of a total liner thickness and no greater than approximately 30% of the total liner thickness (Figure 3, reference 16).

5. Regarding claim 4, Chen et al discloses wherein the portion of the liner is no less than approximately 10% of the total liner thickness and no greater than approximately 20% of the total liner thickness (Figure 3, reference 16).

6. Regarding claim 5, Chen et al discloses wherein the subsequent processing includes: etching through the portion of the liner and the portion of the underlying cap layer to expose a metal layer (Figure 2, reference 5); and forming a via in the opening (Figure 1, reference 12).

7. Regarding claim 6, Chen et al discloses wherein the step of degassing prior to the liner forming step (column 5, lines 50-67 thru column 6, lines 1-17).

8. Regarding claim 7, Chen et al discloses wherein the inert gas is selected from the group consisting of: argon and nitrogen (column 3, lines 64-64).

9. Regarding claim 8, Chen et al discloses, a method of forming a via in a semiconductor device, the method comprising the steps of: first etching an opening through an interlevel dielectric (ILD) layer (Figure 2, reference 4) and partially into an underlying cap layer thereby leaving a remaining portion of the underlying cap layer (Figure 2, reference 6); maintaining the semiconductor device in an inert gas (column 7, lines 32-40); forming a liner at the ILD layer opening and at the remaining portion wherein at least a portion of the liner in the opening is configured to prevent exposure of the ILD layer (Figure 3, reference 16); second etching through the at least a portion of the liner and the remaining portion of the underlying cap layer to expose a metal layer (Figure 3, reference 8); and forming the via in the opening (Figure 1, reference 12).

10. Regarding claim 9, Chen et al discloses the step of degassing prior to the liner forming step (column 5, lines 50-67 thru column 6, lines 1-17).

11. Regarding claim 10, Chen et al discloses wherein the second etching step is conducted in an etching chamber (column 3, lines 52-67).

12. Regarding claim 11, Chen et al discloses wherein the second etching is conducted in a liner deposition chamber (column 3, lines 52-67).

13. Regarding claim 12, Chen et al discloses wherein the remaining portion is no less than approximately 10% of the underlying cap layer thickness and no greater than approximately 90% of the underlying cap layer thickness (Figure 3, reference 6).

14. Regarding claim 13, Chen et al discloses wherein the portion of the liner is no less than approximately 5% of a total liner thickness and no greater than approximately 30% of the total liner thickness (Figure 3, reference 16).

15. Regarding claim 14, Chen et al discloses wherein the portion of the liner is no less than approximately 10% of the total liner thickness and no greater than approximately 20% of the total liner thickness (Figure 3, reference 16).

16. Regarding claim 15, Chen et al discloses wherein the portion of the liner includes tantalum nitride (column 2, lines 50-54).

17. Regarding claim 16, Chen et al discloses a method of forming a via in a semiconductor device the method comprising: the steps of: first etching an opening through an organic interlevel dielectric (ILD) layer (Figure 2, reference 4) and leaving a remaining portion of an underlying cap layer (Figure 2, reference 6) to maintain a metal layer there under sealed (Figure 3, reference 5); maintaining the semiconductor device in an inert gas (column 7, lines 32-

40); degassing the semiconductor device (column 5, lines 50-67 thru column 6, lines 1-17); forming at least a portion of a liner in the opening to prevent exposure of the ILD layer in a chamber (Figure 3, reference 16); second etching through the portion of the liner and the portion of the underlying cap layer to expose the metal layer in the chamber (Figure 3, reference 8); and forming the via in the opening (Figure 1, reference 12).

18. Regarding claim 17, Chen et al discloses wherein the remaining portion is no less than approximately 10% of the underlying cap layer thickness and no greater than approximately 90% of the underlying cap layer thickness (Figure 2, reference 6).

19. Regarding claim 18, Chen et al discloses wherein the portion of the liner is no less than approximately 5% of a total liner thickness and no greater than approximately 30% of the total liner thickness (Figure 3, reference 16).

20. Regarding claim 19, Chen et al discloses wherein the portion of the liner is no less than approximately 10% of the total liner thickness and no greater than approximately 20% of the total liner thickness (Figure 3, reference 16).

21. Regarding claim 20, Chen et al discloses wherein the portion of the liner includes tantalum nitride (column 2, lines 50-54).

Response to Arguments

22. Applicant's arguments with respect to claim 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica D. Harrison whose telephone number is 571-272-1959. The examiner can normally be reached on M-F 7:00am-3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Monica D. Harrison
AU 2813

mdh
February 15, 2006

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